REMARKS

In response to the Final Office Action mailed November 18, 2004, Applicant respectfully requests reconsideration. Claims 1-15 were previously pending in this application. Claims 1, 8 and 9 have been amended. As a result, claims 1-15 are pending for examination with claims 1, 8 and 9 being independent. No new matter has been added. The application as presented is believed to be in condition for allowance.

It should be appreciated that the amendments to claims 1, 8 and 9 are made solely for the purpose of clarification and are not intended to alter the scope of the claims. Thus, these amendments raise no new issues that would require further search and/or consideration.

Telephone Interview With Examiner McCarthy

The undersigned appreciates the courtesies extended to him by Examiner McCarthy during the telephone interview of March 8, 2005. The substance of the telephone interview is summarized below.

Applicant's representatives and Examiner McCarthy discussed the final rejection of claims 1-13 under 35 U.S.C. §102(e) as purportedly being anticipated by Swoboda (U.S. Patent Application Publication No. US2002/0059541). The undersigned briefly summarized the device in Swoboda and the claimed invention.

The undersigned also pointed out that Swoboda illustrates a device that contains an external emulation controller which controlled by an on-chip digital processor. By contrast, the claimed invention includes an emulation device, which is completely on-chip, operable to control the on-chip digital processor. Examiner McCarthy expressed the view that the independent claims of the application in their current form did not clearly require an emulation device, which is completely on-chip, operable to control an on-chip digital processor. Examiner McCarthy stated that if the claims were clarified to clearly recite that the on-chip emulation device is contained entirely on-chip, then the claims would distinguish over Swoboda.

Rejections Under 35 U.S.C. §102

The Office Action has rejected claims 1-13 under 35 U.S.C. §102(e) as purportedly being anticipated by Swoboda (U.S. Patent Application Publication No. US2002/0059541). These rejections are respectfully traversed.

Swoboda discloses an off-chip emulation device which includes on-chip debug facilities ([0059], FIG. 1). The device disclosed by Swoboda offers both bi-directional and unique directional DSP target/host data transfers which are managed by emulation hardware located off-chip ([0039]). The emulation controller disclosed by Swoboda provides a bridge between the host computer and a target system handling all debugging information passed between the debugger application running on the host computer and a target application ([0069]). The off-chip emulation controller also provides debug control ([0080]).

Amended claim 1 is directed to an integrated circuit chip comprising an embedded digital processor and an on-chip emulation device, wherein the on-chip emulation device is contained entirely on-chip, coupled to the digital processor. The emulation device being operable to control the digital processor and to collect information about the operation of the digital processor. The on-chip emulation device having a communication port for off-chip communication, the chip further comprising an on-chip interface having a first port connected to the communication port of the on-chip emulation device, and a second port for connection to a non-proprietary bus. The interface is operable to convert between a format suitable for the on-chip emulation device and a format suitable for the non-proprietary bus.

Claim 1 clearly distinguishes over Swoboda. Claim 1 requires an on-chip emulation device being operable to *control* the digital processor. Swoboda does not teach an on-chip emulation device which is operable to control a digital processor. Swoboda instead teaches on-chip debug facilities controlled by an external emulation device ([0061], [0069]). Therefore, Swoboda fails to teach an on-chip emulation device being operable to control a digital processor, which is required by claim 1. Thus, claim 1 patentably distinguishes over Swoboda such that the rejection of claim 1, as well as claims 2-7 which depend therefrom, under §102(e) is improper and should be withdrawn.

Amended claim 8 is directed to a method of communicating between a remote device and a digital processor. The digital processor being on an integrated circuit chip, the chip having on-chip emulation circuitry, wherein the on-chip emulation circuitry is contained entirely on-chip, for monitoring and controlling the digital processor in response to signals from a remote device. The chip further comprising interface circuitry disposed between a port of the on-chip emulation circuitry and a communication port for the signals. The port is adapted to receive a non-proprietary bus and the non-proprietary bus is adapted to convey signals having a predetermined protocol. The method comprising connecting the non-proprietary bus to the port and to a remote device. The method further comprising receiving the signals from the remote device over the non-proprietary bus in the non-proprietary protocol at the communication port and transferring the signals to the interface circuitry on-chip. The method also comprises the interface circuitry, converting the signals into a form suitable for the on-chip emulation circuitry, and transferring the converted signals to the on-chip emulation circuitry whereby the on-chip emulation circuitry responds to the converted signals to monitor and control the digital processor.

As should be appreciated from this discussion above relating to claim 1, Swoboda does not teach on-chip emulation circuitry for control of a digital processing circuitry. Therefore, claim 8 patentably distinguishes over Swoboda, such that the rejection of claim 8, as well as claims 10-13 that depend therefrom, under §102(e) is improper and should be withdrawn.

Amended claim 9 is directed to a method of debugging a digital processor using a host computer. The digital processor being on an integrated circuit chip and the chip having on-chip emulation circuitry, wherein the on-chip emulation circuitry is contained entirely on-chip, for monitoring and controlling the digital processor in response to signals from the host computer. The chip further comprising interface circuitry disposed between a port of the on-chip emulation circuitry and a communication port for the signals, wherein the port is adapted to receive a non-proprietary bus and wherein the non-proprietary bus is adapted to convey signals having a predetermined protocol. The method comprising connecting the non-proprietary bus to the port and to a host computer. The method further comprises generating the signals in the host computer. The method also comprises receiving the signals from the host computer over the non-proprietary bus in the non-proprietary protocol at the communication port and transferring

the signals to the interface circuitry on-chip. The method further comprising in the interface circuitry, converting the signals into a form suitable for the on-chip emulation circuitry, and transferring the converted signal to the on-chip emulation circuitry whereby the on-chip emulation circuitry responds to the converted signals to monitor and control the digital processor.

As should be appreciated from this discussion above relating to claim 1, Swoboda does not teach on-chip emulation circuitry for control of a digital processing circuitry. Therefore, claim 9 patentably distinguishes over Swoboda, such that the rejection of claim 9 under §102(e) is improper and should be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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